Amendments to Claims

1-51 (canceled)

52. (Currently amended) A method, comprising:

~~creating~~ storing microcode in non-volatile memory in an integrated circuit for causing an embedded processor in the integrated circuit to generate a plurality of pseudo-random test patterns to be used in testing of the integrated circuit;

~~creating~~ storing microcode in the non-volatile memory for causing the embedded processor to move at least one of the plurality of pseudo-random test patterns to a test port register coupled to the embedded processor; and

~~creating~~ storing microcode in the non-volatile memory for causing the embedded processor to move test responses from the test port register to the embedded processor.

53. (Previously presented) The method of claim 52, wherein the testing of the integrated circuit comprises testing a plurality of peripheral devices, the plurality of peripheral devices having associated parallel scan registers coupled to the embedded processor.

54. (Currently amended) The method of claim 52, further comprising ~~creating~~ storing microcode in the non-volatile memory for causing the embedded processor to compact the test responses.

55. (Currently amended) The method of claim 52, ~~wherein the~~ further comprising providing an embedded processor ~~comprises~~ having a plurality of data paths.

56. (Previously presented) The method of claim 55, wherein the testing comprises using the plurality of data paths in a test mode of operation.

57. (Currently amended) The method of claim 52, ~~wherein the~~ further comprising providing a test port register ~~comprises~~ having a plurality of input ports and a plurality of output ports.

58. (Currently amended) The method of claim 53, further comprising ~~creating~~ storing microcode in the non-volatile memory for causing the embedded processor to generate a plurality of deterministic test patterns for the plurality of peripheral devices.

59. (Currently amended) The method of claim 54, wherein ~~creating~~ storing microcode for causing the embedded processor to compact the test responses comprises ~~creating~~ storing microcode in the non-volatile memory to cause the embedded processor to:

move a first test response into a first accumulator;

add a first signature to the first accumulator;

move a second test response into a second accumulator;

output the content of the first accumulator; and

add the output of the first accumulator into the second accumulator.

60. (Currently amended) The method of claim 59, wherein ~~creating~~ storing microcode for causing the embedded processor to compact the test responses further comprises ~~creating~~ storing microcode in the non-volatile memory to cause the embedded processor to:

move the second test response into the first accumulator;

add a second signature into the first accumulator, the second signature comprising the first test response;

move a third test response into the second accumulator; and

add the output of the first accumulator into the second accumulator.

61. (Currently amended) One or more computer-readable media having computer-executable instructions for performing a ~~the~~ method ~~of claim 52~~ comprising:

storing microcode in non-volatile memory in an integrated circuit for causing an embedded processor in the integrated circuit to generate a plurality of pseudo-random test patterns to be used in testing of the integrated circuit;

storing microcode in the non-volatile memory for causing the embedded processor to move at least one of the plurality of pseudo-random test patterns to a test port register coupled to the embedded processor; and

storing microcode in the non-volatile memory for causing the embedded processor to move test responses from the test port register to the embedded processor.

62. (Currently amended) An apparatus, comprising:

means for generating pseudo-random test patterns in an integrated circuit, wherein the integrated circuit comprises an embedded processor core and a plurality of peripheral devices, the embedded processor core comprising a plurality of data paths, and wherein the means for generating pseudo-random test patterns comprises multiplying n least significant bits of a 2n-bit pseudo-random number generated in an immediately preceding iteration and stored in a first register, with an n-bit multiplier constant stored in a second register to produce a 2n-bit product;

means for testing the plurality of peripheral devices using the pseudo-random test patterns and the plurality of data paths; and

means for compacting peripheral device test-response data.

63. (Previously presented) The apparatus of claim 62, wherein the embedded processor core comprises a plurality of registers, at least one multiplier, at least one adder, and at least one accumulator.

64. (Previously presented) The apparatus of claim 62, wherein the integrated circuit further comprises a test port register, the test port register serving as an interface between the embedded processor core and at least one scan register.

65. (Canceled)

66. (Currently amended) The apparatus of claim ~~65~~ 62, wherein the means for generating pseudo-random test patterns further comprises adding the 2n-bit product to n most significant bits of the 2n-bit pseudo-random number stored in n least significant locations of an accumulator with 2n locations to produce a new 2n-bit pseudo-random number for a current iteration.

67. (Previously presented) The apparatus of claim 66, wherein the means for generating pseudo-random test patterns further comprises outputting n least significant bits of the new 2n-bit pseudo-random number as an n-bit pseudo-random test vector for the plurality of peripheral devices.

68. (Previously presented) The apparatus of claim 62, wherein the means for compacting peripheral device test-response data comprises:

means for moving an n-bit segment of the peripheral device performance data to a first-stage accumulator;

means for adding the n-bit segment to a signature value at the first-stage accumulator;

means for cascading the signature value to a second-stage accumulator; and

means for adding the n-bit segment to the cascaded result.

69. (Previously presented) The apparatus of claim 68, wherein the means for cascading the signature value to the second-stage accumulator comprises a 1's complement convention.

70. (Previously presented) The apparatus of claim 68, wherein the means for cascading the signature value to the second-stage accumulator comprises a rotate carry scheme.

71. (Previously presented) A method for testing integrated circuits, comprising:

a step for producing at least one two-dimensional pseudo-random test pattern in an integrated circuit, the integrated circuit having an embedded processor and a peripheral device;

a step for generating at least one two-dimensional deterministic test pattern in the integrated circuit;

a step for testing the peripheral device using the two-dimensional pseudo-random test pattern and the two-dimensional deterministic test pattern; and

a step for compacting test-response data.

72. (Previously presented) The method of claim 71, wherein the step for testing the peripheral device comprises a step for providing the two-dimensional pseudo-random test pattern and the two-dimensional deterministic test pattern to the peripheral device via a test port register, the test port register coupled to the embedded processor and at least one scan register.

73. (Previously presented) The method of claim 71, further comprising a step for repeating the step for testing the peripheral device until all desired test patterns have been produced and used in the testing.